

REQUEST
FOR
CONTINUED EXAMINATION (RCE)
TRANSMITTAL

Section (b) of 35 U.S.C. § 132, effective on May 29, 2000,
provides for continued examination of an utility or plant application
filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA)

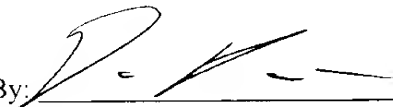
Application Number	09/943,324
Filing Date	August 30, 2001
First Named Inventor	Kie Y. Ahn et al.
Group Art Unit	2818
Examiner Name	Phuc T. Dang
Attorney Docket Number	303.678US3

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application entitled
STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES.

Submission required under 37 C.F.R. § 1.114

1. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on ☐
2. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ☐
3. ☒ An Amendment Under 37 CFR § 1.116 (5 pages) is enclosed.
4. ☐ A new power of attorney (☐ pages) is enclosed.
5. ☒ An Information Disclosure Statement is enclosed (1 page)
 - a. 1 Form(s) 1449
 - b. 5 Copies of IDS Citations
6. ☒ A check in the amount of \$750.00 is attached to pay the RCE filing fee required under C.F.R. § 1.17(e).
7. ☒ The Commissioner is hereby authorized to credit overpayments or charge any fees set forth in 37 C.F.R. §§
1.16 through 1.18 to Deposit Account No. 19-0743.
8. ☐ A petition for extension of time in the prior application (☐ pages) is enclosed along with a check in the amount of \$
to pay the extension fee.
9. ☒ Other: Clean Version of Pending Claims (7 pages)

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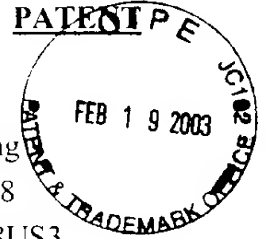
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service
with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Box RCE, Washington, D.C. 20231,
on this 12th day of February, 2003.

Name Amy Moriarty

Signature Amy Moriarty

EXPEDITED PROCEDURE – EXAMINING GROUP 2818

S/N 09/943324



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.

Examiner: Phuc Dang

Serial No.: 09/943324

Group Art Unit: 2818

Filed: August 30, 2001

Docket No.: 303.678US3

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

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Commissioner for Patents
Washington, D.C. 20231

In response to the amended final Office Action faxed January 10, 2003, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 33, 55, 62, 67, 73, 78, 82, and 86. The specific amendments to individual claims are detailed in the following marked up set of claims.

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33. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the first transistor includes a dielectric layer of a first thickness, including a top layer which exhibits a high resistance to oxidation at high temperatures, separating a gate from the channel region; and

a second transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the second transistor includes a dielectric layer of second thickness different from the first thickness, separating a gate from the channel region.

55. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes: